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ABSTRACT OF THE DISCLOSURE:

The present invention proposes a improved transistor with π -gate structure usable at microwave and millimeter wave and a method for producing the same.

According to one aspect of the invention or the method, there is provided a manufacturing method of gate with π -structure by using an air bridge technique comprises: the step of vapor-depositing, on a wafer 2, to form a drain 5 and source layers 3 of Ti/Au as the primary metal layers in the thickness of 200 Å/4000 Å through PHEMT process; the step of forming silicon nitride film 9 in the thickness of 1000 Å, patterning the formed silicon nitride film 9 by using an electron beam exposure device, forming gate foot steps by etching the film, and then conducting HMDS coating by PR-via pattern forming process using the positive photo irradiation drawing process, conducting AZ1518 coating at 2000 rpm for 20 seconds, conducting soft-baking at 98℃ for 45 seconds, aligning patterns, conducting UV exposure and developing for 1 minute and 30 seconds, and subsequently conducting a hard-baking at 115℃ for 4 minutes and 30 seconds to thereby harden the resist 7; the step of forming, by vapor-depositing, a thin gold film 8 in the thickness of about 250~300 Å on the surface of GaAs wafer 2; the step of conducting HMDS coating after forming secondary metal patterns 7a by using an image inversion process, conducting AZ5214E coating at 2000 rpm for 10 seconds, conducting soft-baking at 98℃ for 45 seconds, aligning patterns, and then conducting free exposure for 7 seconds, reverse baking at 110℃ for 50 seconds and plot exposure for 25 seconds before development; the step of disconnecting the source 3 and drain 5 by etching off the exposed gold film 8 by using the metal etching solution consisting of N, KCN, H_2O at the volume ratio of 10 : 500 : 100, and thereafter forming a gate 4 in the thickness of 200 Å/8000 Å by vapor deposition of Ti/Au and attaining a finished gate 4 with π -structure through lifting-off by means of acetone; and the step of performing the process of back side via-hole 10 on the wafer 2 to ground the GND 1 to the source layer 3.

The transistor with π -gate structure according to the invention is improved in

noise characteristic because of low electric resistance which is brought up by the structure of gate straddling above the drain stage. (Figure 2).